



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,936	08/18/2003	Naoyuki Koizumi	CU-3332 RJS	4286
26530	7590	04/05/2005	EXAMINER	
LADAS & PARRY LLP 224 SOUTH MICHIGAN AVENUE SUITE 1200 CHICAGO, IL 60604			DOTY, HEATHER ANNE	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

A1

Office Action Summary	Application No.	Applicant(s)	
	10/642,936	KOIZUMI, NAOYUKI	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 23 March 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-5 is/are rejected.
 7) Claim(s) 1 is/are objected to.
 8) Claim(s) 6-8 are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 18 August 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>8/18/03, 2/28/05</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: In line 16, remove the last word, "the". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (U.S. 5,904,546) in view of Coleman (U.S. 4,729,971).

With respect to claim 1, Wood et al. teaches a method of fabricating a semiconductor chip from a semiconductor wafer having a first surface (14 in Fig. 1) supporting a semiconductor element and a second surface opposite the first surface (18 in Fig. 2), the method comprising the steps of: performing anisotropic etching on a remaining portion of the cutting portion from one or both of the first surface and the second surface, thereby cutting the cutting portion of the semiconductor wafer (column 4, lines 21-23, 49-53; Fig. 3).

Wood et al. does not teach performing isotropic etching at least partially on a cutting portion of the semiconductor wafer from one or both of the first surface and the second surface.

Coleman teaches a method of fabricating a semiconductor chip from a semiconductor wafer comprising performing isotropic etching at least partially on a cutting portion of the semiconductor wafer (column 3, lines 44-45) from a first surface (column 2, line 5) to give smooth edges (abstract).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the methods of Coleman and Wood et al. to perform isotropic etching at least partially on a cutting portion of the semiconductor wafer, as taught by Coleman, and then perform anisotropic etching on a remaining portion of the cutting portion, thereby cutting the cutting portion of the semiconductor wafer, as taught by Wood et al. The motivation for doing so at the time of the invention would have been to give the etched surface sloped sidewalls (Wood et al., column 3, line 65) on one portion and smooth sidewalls (Coleman, abstract) on another portion.

With respect to claim 2, Coleman and Wood et al. together teach the method as claimed in claim 1. Coleman further teaches forming a resist on the first surface to expose the cutting portion on the first surface, when the cutting portion is isotropically etched from the first surface (column 3, lines 23-27).

With respect to claim 4, Coleman and Wood et al. together teach the method as claimed in claim 1. Wood et al. further teaches forming a resist on the second surface to expose the cutting portion on the second surface (etch mask **24** in Fig. 3A; column 3, lines 42-43). As noted above, Coleman teaches that the cutting portion is isotropically etched. Therefore, it would be obvious to combine the teachings of Coleman and Wood et al. to arrive at the invention as specified in claim 4, for the reasons discussed above.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (U.S. 5,904,546) in view of Coleman (U.S. 4,729,971) as applied to claims 2 and 4 above, and further in view of Bunch et al. (U.S. 2002/0145827).

With respect to claims 3 and 5, Wood et al. and Coleman together teach the method as claimed in claim 2—as further limited by claim 3—and claim 4—as further limited by claim 5. They do not teach that the resist has rounded-off corners.

Bunch et al. teaches etching a silicon substrate using a resist with rounded-off corners to produce a surface with rounded edges (page 4, claim 20).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the rounded-off resist pattern taught by Bunch et al. as an etch mask for the isotropic etch taught by Coleman and the anisotropic etch taught by Wood et al. to arrive at the invention as specified in claims 3 and 5. The motivation for doing so at the time of the invention would have been to achieve a surface with rounded edges, as expressly taught by Bunch et al.

Election/Restrictions

Applicant's election without traverse of claims 1-5 in the reply filed on 3/23/05 is acknowledged.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wegleiter et al. (U.S. 5,972,781) teaches a method of dicing a semiconductor wafer by an initial anisotropic etch from a surface supporting a semiconductor element followed by an isotropic etch from the opposite surface that fully cuts the wafer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig A. Thompson
CRAIG A. THOMPSON
PRIMARY EXAMINER